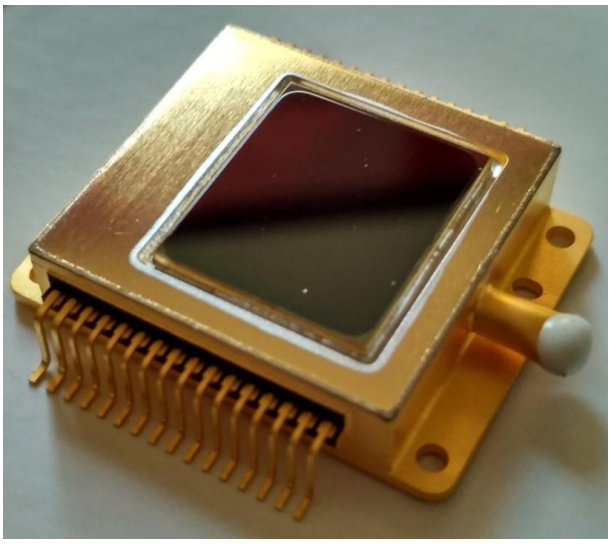

IR 03 18 X2A 640×512 17μm

Uncooled LWIR Microbolometer Focal Plane

Datasheet Version 2.0

Ecor Tech Co.,Ltd.

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CONTENTS

1 DESCRIPTION

IR 03 18 X2A is a highly reliable uncooled infrared focal plane array (IRFPA) detector for thermal imaging with high sensitivity, small size, light weight and low power. It is a device sensitive to the radiation in the infrared range (LWIR, 8-14μm) of the spectrum, also called *thermal radiation*.The focal plane has an array of pixels, which are made of VO_x resistive microbolometers connected to the silicon readout integrated circuit (ROIC). The entire chip is assembled with a thermal electric cooler (TEC) inside a metal vacuum housing.

This datasheet does not intend to give a step-by-step instruction to develop imaging modules. It only provides the necessary configuration information, method and drawings. A concrete goal is to have a uniform output under uniform irradiation.

It has the following features and specifications.

Array format	640$\times$512
Pixel pitch	17$\times$17μm
Max frequency	60Hz
Spectral range	8~14μm
NETD	<40mK
Typical responsivity	15mV/K
Power supply	5V (analog), 3.3V/ 5V for digital
Digital input	3.3V
Output	2 analog
Output dynamic range	> 70dB
Readout Mode	rolling shutter
Package	metal, 32 pin
Cooler	TEC
Integration time	Adjustable

2 ELECTRICAL INTERFACE

Fig.1 shows the pin labeling of the detector. Tab.1 gives a description of the I/O pins, and 2 gives out a typical implementation scheme.

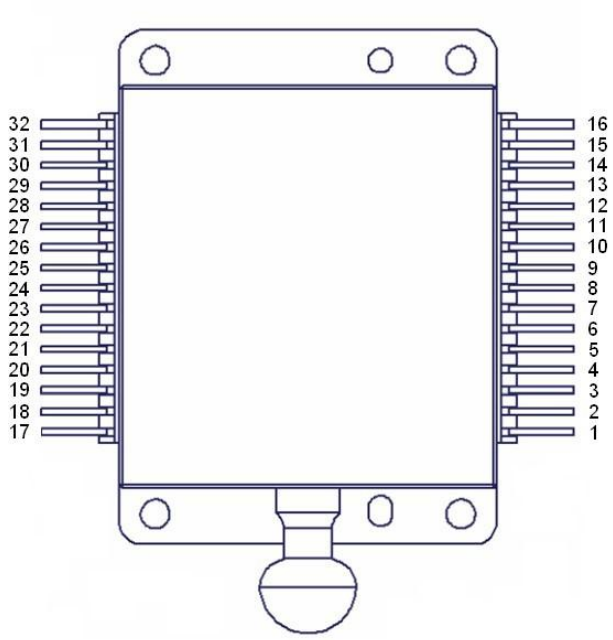

Figure 1: IR 03 18 X2A I/O pin number

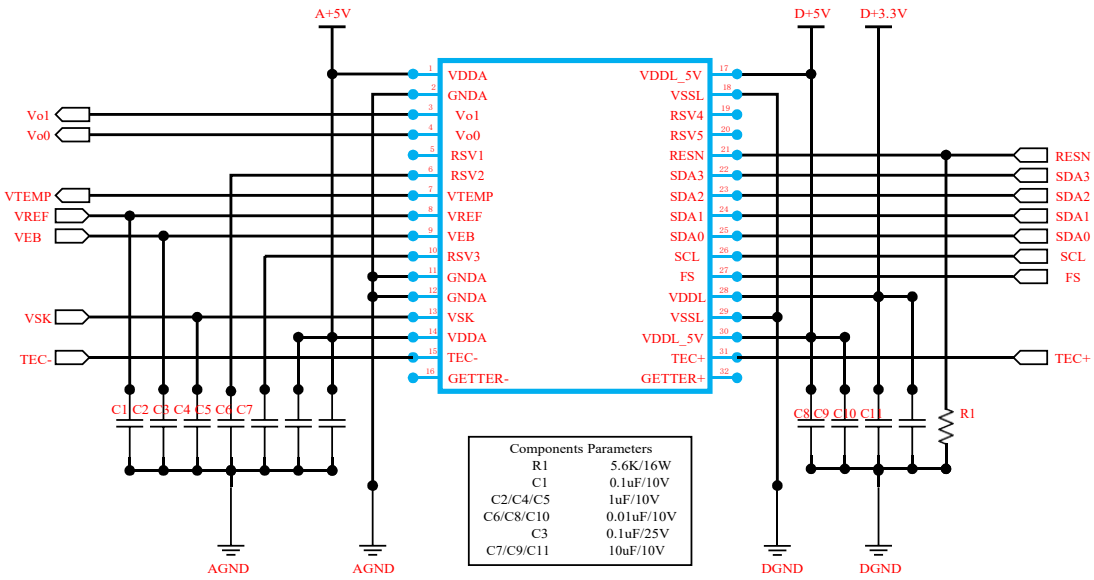

Figure 2: IR 03 18 X2A typical implementation

Table 1: IR 03 04 X2A pin description

PIN #	Symbol	Description
1	VDDA	Analog power supply
2	GNDA	Analog ground
3	Vo1	Analog video output Vo1
4	Vo0	Analog video output Vo0
5	RSV1	Reserved pin, left floating
6	RSV2	Reserved pin, connect the 1uF capacitor to the analog ground
7	VTEMP	Analog output signal that gives the FPA temperature
8	VREF	Reference voltage
9	VEB	Microbolometer bias voltage
10	RSV3	Retain the pin and connect the 1uF capacitor to the analog ground
11	GNDA	Analog ground
12	GNDA	Analog ground
13	VSK	Bias voltage
14	VDDA	Analog power supply
15	TEC-	TEC negative input
16	GETTER-	Getter connection
17	VDDL_5V	Digital power supply
18	VSSL	Digital Ground
19	RSV4	Reserved pin, left floating
20	RSV5	Reserved pin, left floating
21	RESN	Power-on reset signal
22	SDA3	Serial input bus 3
23	SDA2	Serial input bus 2
24	SDA1	Serial input bus 1
25	SDA0	Serial input bus 0
26	SCL	Detector input master clock
27	FS	Frame synchronization signal
28	VDDL	Digital power supply
29	VSSL	Digital Ground
30	VDDL_5V	Digital Power Supply
31	TEC+	TEC positive input
32	GETTER+	Getter connection

2.1 INPUT VOLTAGE

The input voltage of the ROIC includes:

VDDA Analog power supply
GNDA Analog ground
VDDL_5V Digital power supply
VDDL Digital power supply
VSSL Digital Ground
VSK Bias voltage
VEB Bias voltage
VREF Bias voltage

The requirement of the ROIC bias voltage are shown in Tab.2.

Table 2: Requirements for ROIC input voltage

Input	Fixed	Value(@300K)	Range	I_{max}	RMS noise
VDDA	Y	5V±50mV	-	70mA	30uV(1Hz ~ 50kHz)
GNDA	Y	0V ±25mV	-	-	Analog ground
VDDL_5V	Y	5V ± 50mV	-	15mA	30uV(1Hz ~50kHz)
VDDL	Y	3.3V ±300mV	-	5mA	60uV(1Hz ~50kHz)
VSSL	Y	0V ±300mV	-	-	Digital ground
VSK	N	4.5V	4.4 ~5.0V	30mA	30uV(1Hz ~50kHz)
VEB	Y	1.9V	-	1mA	30uV(1Hz ~50kHz)
VREF	Y	2.5V	-	1mA	30uV(1Hz ~50kHz)

2.2 DIGITAL INPUT SIGNAL

Digital input signals include ***FS*** ,***SCL*** ,***SDA0*** ,***SDA1*** ,***SDA2*** and ***SDA3*** and ***RESN*** . The low level of the digital input signal is 0 ± 300mV, while the high level signal is 3.3V ± 300mV. The input timing sequence is shown in Fig.3.

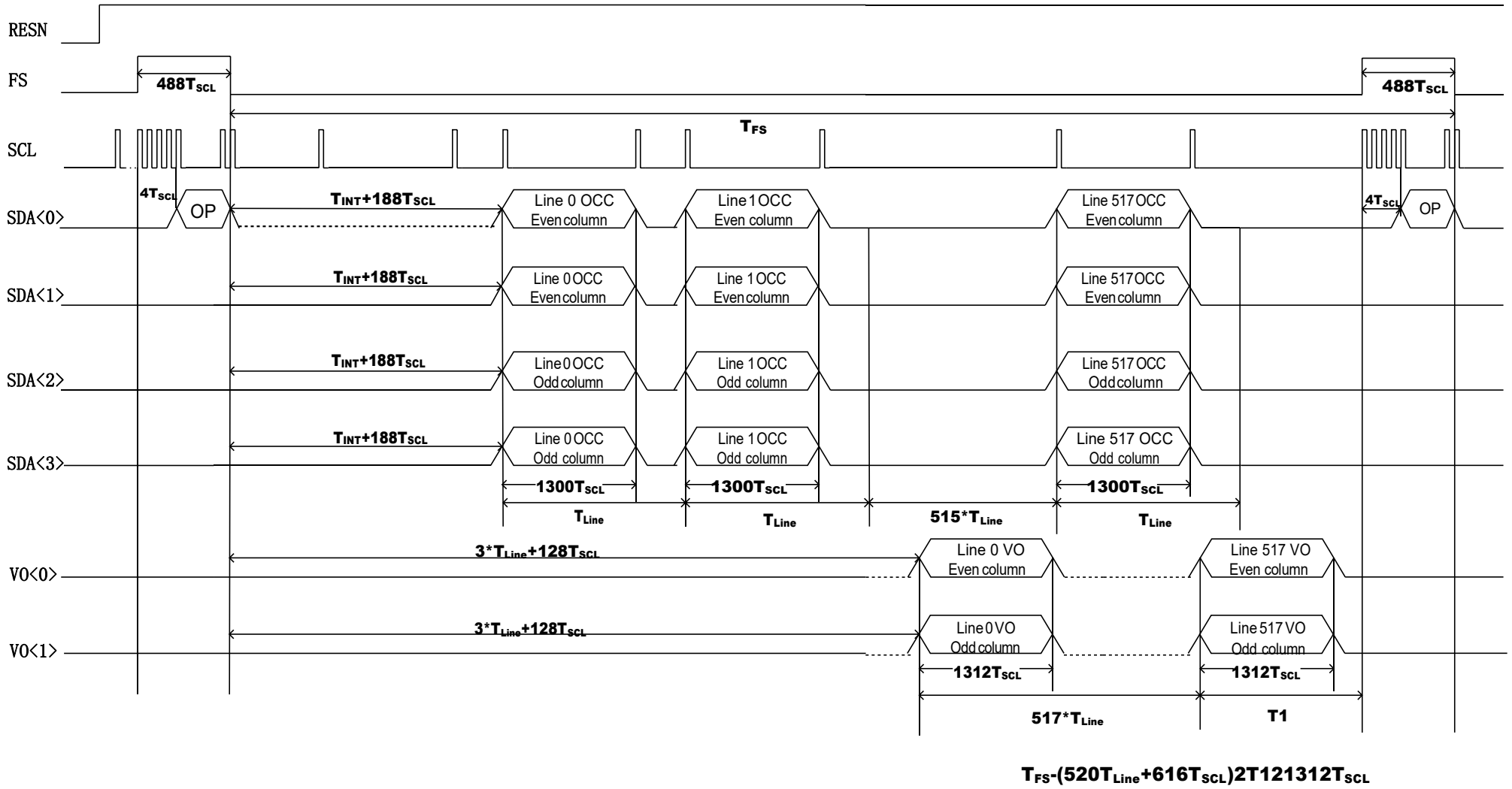

Figure 3: Timing sequence diagram (SyncData<5:0>=*,aOOOOOO*)

2.2.1 | *SCL*

SCL is the input master clock, which controls the serial input data(***SDA<3:0>***), the detector output(***Vo<1:0>***), and the the frame signal(***FS***) cycle. The typical frequency is 40MHz and the duty cycle is 50%. The maximum frequency of ***SCL*** is 47MHz.

2.2.2 | *FS*

FS is the frame signal, which represents the beginning of a frame, and its period is equivalent with a frame period, typically 20ms (for 50Hz) and at most 16.67ms (for 60Hz). The high level width of ***FS*** is $488T_{SCL}$. At this level, the chip transmits the operation mode data, whose edge is aligned with the rising edge of ***SCL*** . One frame requires a minimum of $520T_{Line}$ + $1928T_{SCL}$, which is about 522 rows.

2.2.3 | *RESN*

RESN is the power-on reset signal. It is a low-level pulse (active-low) whose width is not less than 1μs. After power-on, ***RESN*** holds high during the operation period.

2.2.4 | *SDA<3:0>*

SDA<3:0> is a serial input bus for transmitting operating mode data and E-OCC data. OCC is the acronym for on chip correction. When ***FS*** is at the high level, ***SDA0*** inputs 121 bits of operation mode data, which appears $4T_{SCL}$ after the ***FS*** rising edge. The width of each bit is $4T_{SCL}$. At T_{INT} + $188T_{SCL}$ after the ***FS*** falling edge, the OCC data starts to be transmitted and ***SDA<3:0>*** sends 518 rows of OCC correction data, updated once for each row, with each bit being T_{SCL} wide. At the same time, the serial data bus ***SDA<3:0>*** has the OCC correction data of two adjacent columns (2 pixels) of the same row. ***SDA0*** and ***SDA1*** transmit the $2N^{th}$ column OCC data, and ***SDA2*** and ***SDA3*** transmit
the $2N + 1^{th}$ column of data ($323 > N > 0$), in total of 648(0-647) columns of E-OCC data.

The 648^{th} column is the Em-OCC of the mirror circuit, which is used to correct the frame mean. The larger is the 8 bits DAC value, the larger is Vo.

The 649^{th} column is row replacement selection data, updated for each row. R<1:0> defaults to send b'10. The user can use this data to replace a defect row.

It takes $1300T_{SCL}$ of time to transmit a total of 650 columns of OCC per line.

The OCC data for each pixel has 8 bits. ***SDA1*** and ***SDA3*** transmit the

higher 4 bits, and ***SDA0*** and ***SDA2*** transmit the lower 4 bits. Therefore, ***SDA0*** ,

SDA1 , ***SDA2*** , and ***SDA3*** each contains 4 bits of OCC data during one pixel time.

Fig.4 shows the OCC code transmission format. Each pixel has 8 bits of E-OCC code. Each row sends data from column 0 to 647, wherein E3[2] representing the 3^{rd} OCC bit of column 2 of E-OCC data.

Among the 8 bits of E-OCC data of each pixel, the higher 5 bits are used to coarsely adjust Vo and the lower 3 bits for fine adjustment. Vo is smaller when E-OCC DAC value is larger. The typical integration time is $30us$ and the normalized gain is 1.00. One LSB of the coarse adjustment is 140mV, and 17.5mV for the fine adjustment.

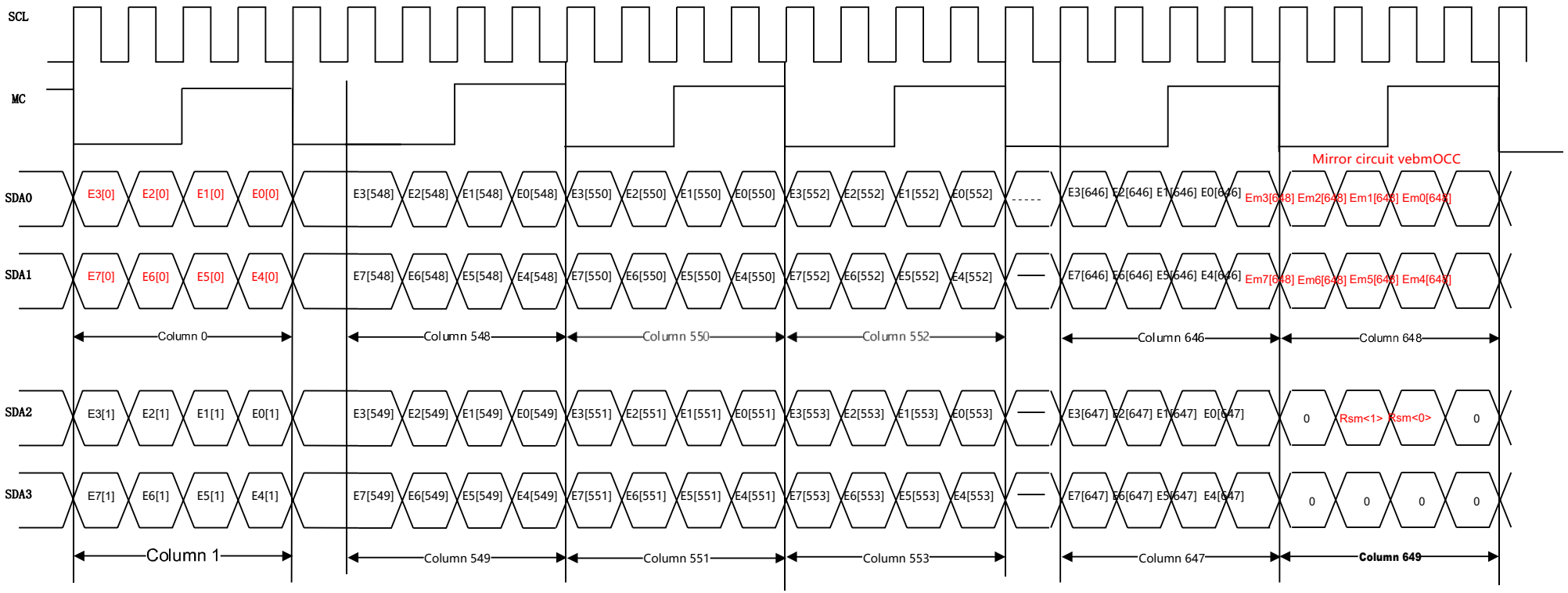

Figure 4: OCC data transmission format

2.2.5 | *Vo<1:0>*

Vo<1:0> is the two analog outputs of the detector. The output data width of one pixel is $4T_{SCL}$. The output data is updated on the rising edge of ***SCL***.

The output range is $0.5V - 4.5V$. The load capacitance should not exceed 40pF and the load resistance not lower than 100kΩ.

IR 03 18 X2A can output 518 rows and 656 columns of data, but the first 2 rows and the last 8 columns act as nonessential, and therefore the effective output is 516 rows and 648 columns. The user can choose an effective $512x640$ central area to output as he see fits.

The line synchronization data ***SyncData<5:0>*** in the operation mode is to control how long after the FS falling edge the effective output of ***Vo<1:0>*** can start.

During the same pixel output time, the data on ***Vo0*** and ***Vo1*** are of the adjacent columns. ***Vo0*** outputs the data of even columns counting from 0, and ***Vo1*** outputs the data of odd columns counting from 1. The data of ***Vo<1:0>*** is output row by row, but the data of the last line only needs $1312T_{SCL}$ to complete the output.

The user needs to pay attention to the detector's analog output ***Vo<1:0>***, it takes a certain settling time. There will be a delay in the actual stable output time, so the sampling time also needs a corresponding delay. Fig.5 is the recommended moments for sampling.

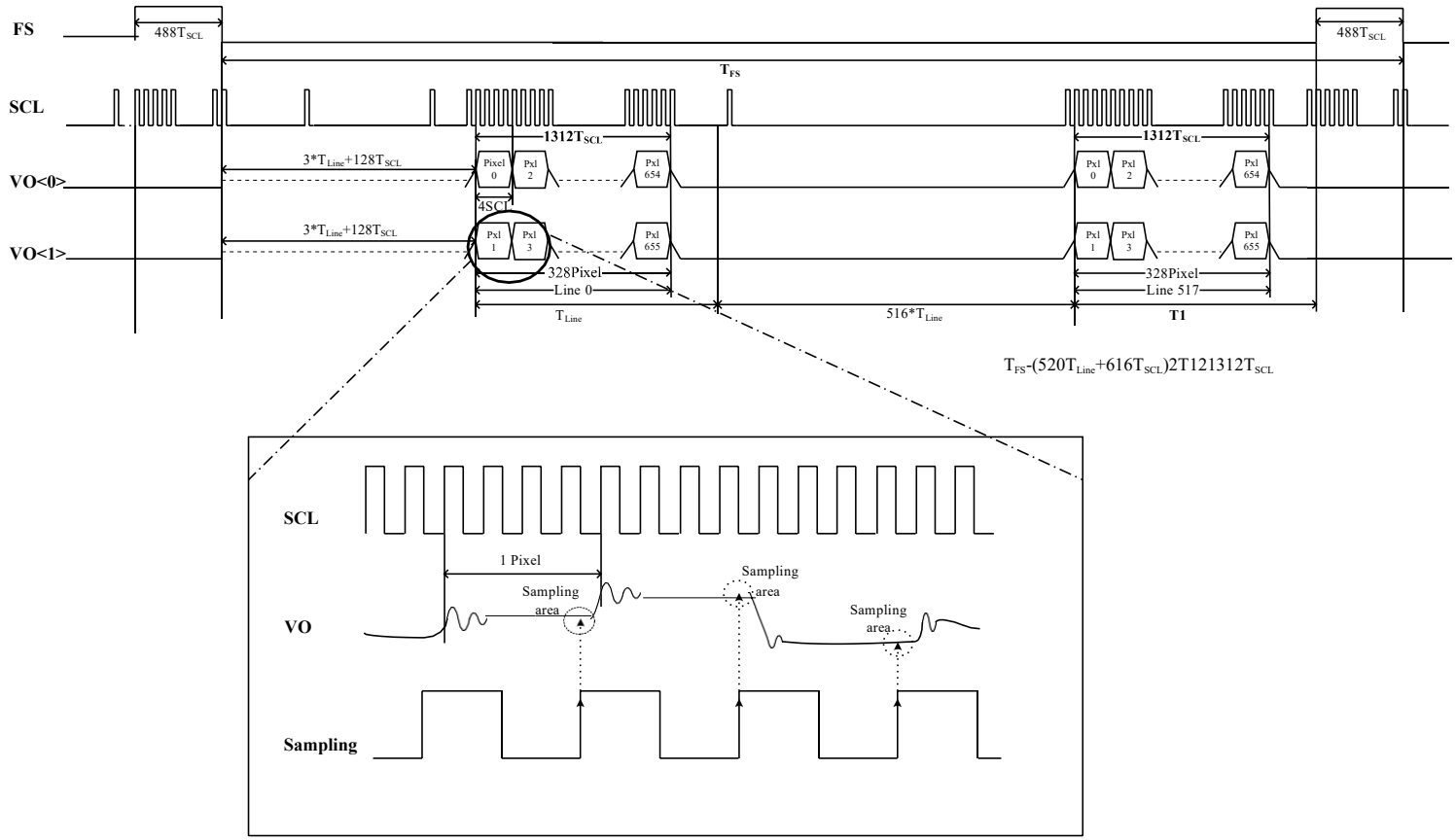

Figure 5: FS, SCL and output ***Vo<1:0>*** relationship and Vo output and sampling recommendation (***SyncData<5:0>***=,a000000)

2.3 DETECTOR CONFIGURATION

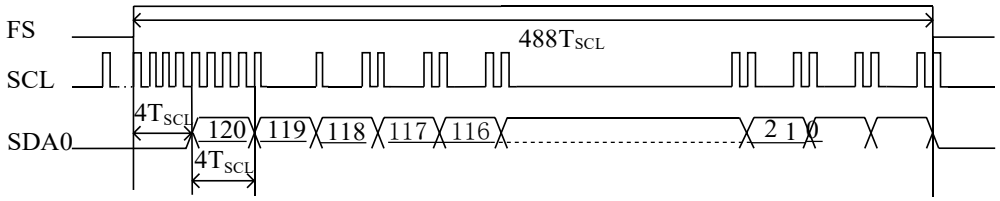

Figure 6: transmission time sequence of detector configuration data

As shown in Fig.6, ***FS*** holds high for $488T_{SCL}$ to transmit the 121 bits of configuration data, which is updated on the rising edge of ***SCL*** . Operation data appears on ***SDA0*** occur at $4T_{SCL}$ after the ***FS*** rising edge. Each data is $4T_{SCL}$ wide.

The operating mode data of IR 03 18 X2A has 121 bits in total, which are decomposed as shown in Tab.3. The reserved flag bits should not be changed at will to avoid malfunction or even damage of the detector. The data transmission follows the principle of *higher-bit-first*. The user can modify the detector integration time, row cycle, row synchronization and the integration capacitance through the SDA0 pin. The operating mode data will be provided to the customer in 128 bits, i.e., 16 hexadecimal numbers. To obtain the 121-bit operating mode data, the user needs to convert it into binary form and remove the highest 7 bits.

Table 3: IR 03 18 X2A operating mode data decomposition

Mode_data Bits	Function	Value	Modification
<120:119>	Reserved	-	-
<118:116>	Gain<2:0>	011	USER
<115:92>	Reserved	-	-
<91:84>	PTCR<7:0>	-	USER
<83:79>	NTCR<4:0>	-	USER
<78:73>	P_f<5:0>	-	USER
<72:55>	P_c<17:0>	-	USER
<54:47>	Reserved	-	-
<46:44>	Set_OCC<2:0>	100	USER
<43>	Reserved	-	-
<42>	Set_veb<0>	1	USER
<41>	Set_vref<0>	1	USER
<40:20>	Reserved	-	-
<19:10>	Tline_data<9:0>	0101110010	USER

<9:0>	Tline_data<9:0>	010010 1100	USER

2.3.1 | RESERVED CONFIGURATION BITS

The reserved configuration bits (mode_data<120:119>, mode_data<115:92>, mode_data<54:47>, mode_data<43>, mode_data<40:20>) are the configuration of the chip's internal circuit module. They MUST be configured in accordance with the factory test report provided to the customer.

2.3.2 | GAIN

The operation mode data mode_data<118:116> are the control bits of the detector gain (Gain<2:0>). By changing these three bits, the user can select the corresponding gain according to Tab.4.

Table 4: Configuration of gain: Gain<2:0>

mode_data<118>	mode_data<117>	mode_data<116>	normalized gain
0	0	0	2.00
0	0	1	1.50
0	1	0	1.20
0	1	1	1.00
1	0	0	0.86
1	0	1	0.75
1	1	0	0.67
1	1	1	0.60

2.3.3 | OUTPUT DRIFT ADJUSTMENT DUE TO TEMPERATURE CHANGE

The operation mode data mode_data<91:79> is the adjustment parameter for detector output drift coefficient due to temperature change. Mode_data<91:84> is the 8-bit positive temperature coefficient adjustment parameter PTCR<7:0>, and mode_data<83:79> is the 5-bit negative temperature coefficient adjustment parameter NTCR<4:0>. The user can use the provided data, or choose to configure on his own.

When the Vo frame average increases as the temperature goes up, it is called as *positive temperature drift*. The greater the mean value of the Vo frame per unit temperature changes, the greater the positive temperature drift is. In operation, the greater the value of PTCR<7:0> the user adjusts to, the greater the positive temperature drift is, as shown in Fig.7.

When the Vo frame average decreases as the temperature goes up, it is called as *negative temperature drift*. The greater the mean value of the Vo frame per unit temperature changes, the greater the negative temperature drift is. In operation,

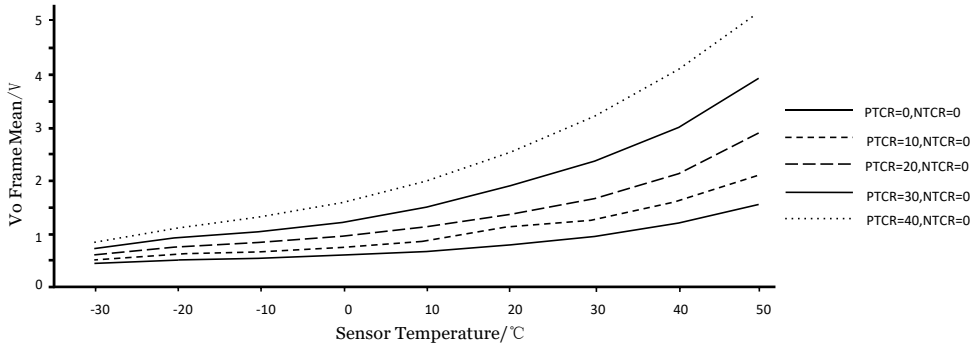

Figure 7: Schematic diagram of positive temperature drift coefficient adjustment

the greater the value of NTCR<7:0> the user adjusts to, the greater the negative temperature drift is, as shown in Fig.8.

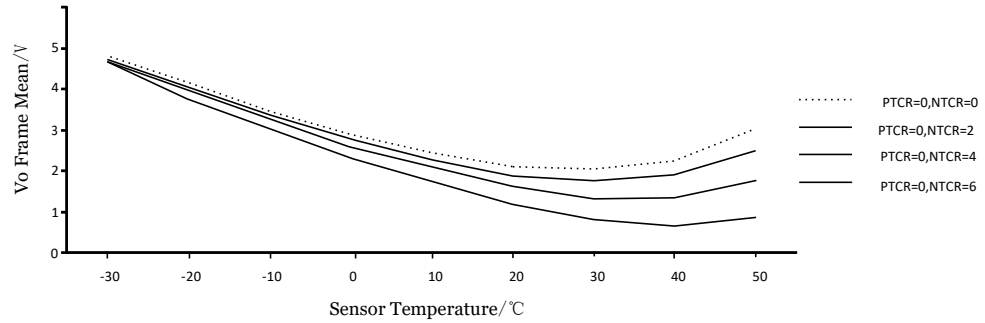

Figure 8: Schematic diagram of negative temperature drift coefficient adjustment

During the tuning process, the temperature coefficient adjustment parameters need to be determined according to the specific conditions of the detector. In general, if the positive temperature drift is large, the user needs to increase the value of NTCR<4:0>; if the negative temperature drift is large, then increase the value of PTCR<7:0>.

2.3.4 OUTPUT FRAME MEAN ADJUSTMENT

To adjust the frame mean, the coarse adjustment can be performed first and then finely tune it to close in on the preset value.

Mode_data<78:55> is the parameter to adjust the detector frame mean. During the OCC process, the global circuit overall output is adjusted to the preset value. The data switch is toggled. 0 means ON, 1 means OFF. By adjust- ing these 24 bits, the user can confine the output of most of the pixels between 1 −4V.

Mode_data<72:55> is the parameter for coarse tuning. These 18 bits of data carry no weight. The more zeroes in the data, the lower the output.

Mode_data<78:73> is the parameter for fine tuning. The value of the 6-bit code is from 00 0000 to 11 1111, and the frame mean gradually increases along. It is important to note that the highest bit of mode_data<78:73> is bit 73 and the lowest is bit 78.

For the specific adjustment method, refer to subsubsection 2.5.1.

2.3.5 E-OCC PRECISION ADJUSTMENT

Mode_data<46:44> are the control bits (E_Sel<2:0>) for selecting the E-OCC correction range (adjustment accuracy) during OCC process. The user is recommended to use the provided data. In case of necessary recalibration, he can use Tab.5 to find the appropriate E-OCC settings.

Table 5: Configuration of E-OCC adjustment accuracy

mode_data<46>	mode_data<45>	mode_data<44>	Accuracy
0	0	1	0.25
0	1	0	0.50
0	1	1	0.75
1	0	0	1.00
1	0	1	1.25
1	1	0	1.50
1	1	1	1.75

2.3.6 LINE TIME DATA

Mode_data<19:10>, also in the name of Line_data<9:0>, sets the line time. It is in unit of $4T_{SCL}$. IR 03 18 X2A has dual port output. The minimum line time is $1432T_{SCL}$, and the maximum can be calculated by frame frequency and T_{SCL}. The user can use the provided data or configure on his own according to Tab.6.

The decimal numbers in the second column of Tab.6 and 7 are just the corresponding binary numbers in the first column multiplied by four.

2.3.7 INTEGRATION TIME

Mode_data<9:0>, also in the name of Tint_data<9:0>, sets the integration time. It is in unit of $4T_{SCL}$. The minimum integration time is $132T_{SCL}$, and the maximum is the line time minus $176T_{SCL}$. The user can use the provided data

Table 6: Allocation of line time

Line_data(mode_data<19:10>)	Line time
0101110000	
0101100110	$1432T_{SCL}$
0101111100	$1520T_{SCL}$
…	…
0110000000	$1536T_{SCL}$
…	…

or configure on his own according to Tab.7

Table 7: Allocation of integration time

Tint_data(mode_data<9:0>)	Definition
0001010000	$320T_{SCL}$
0001000000	$256T_{SCL}$
0001100000	$384T_{SCL}$
0001110000	$448T_{SCL}$
0010000000	$512T_{SCL}$
0010010000	$576T_{SCL}$
0100000000	$1024T_{SCL}$
…	…

2.4 OCC OF DETECTOR

There are 518 rows of OCC data, with each row containing data for 650 columns. Since for each column 8 bits are used, a total of 5200 bits of OCC data are transmitted in one line time. Each of the four serial data lines transmits 1300 bits, and the width of one bit $1T_{SCL}$. In each frame, the serial data bus SDA<3:0> needs to transmit a total of 518 lines of OCC data.

The user is recommended to use the provided data (★ *occ becd.c_t*) for room temeprature OCC. In case of non-uniform output, the user needs to follow the method described in the next subsection if he chooses to configure on his own.

2.5 THE ANALOG OUTPUT ADJUSTMENT METHOD

The contents of this subsection are for advanced users.

OCC data of a detector depend on many factors from the module condi-

tions, such as clock frequency, integration time. Therefore, the provided E-OCC data may not fit all imaging systems and the customer sometimes need to adjust it on his own. The goal of this subsection is that, after the operation mode and bias voltage are well configured, the analog output (usually named as Vo) of the dominant majority of all pixels, should be stable within $2.0\text{V} \pm 300\text{mV}$ or $_{2.5}$ V $\pm$ 300mV under uniform room temperature irradiation.

2.5.1 | PRELIMINARY ADJUSTMENT

After the user loaded the provided configuration and E-OCC data, if the analog output of the dominant majority of all pixels are between 1 –4V, then pre-adjustment is not needed. As a convention, Vo is defined as super-saturation if it is greater than 4.5V or under-saturation if it is less than 0.5V.

The loaded detector configuration data has 121 bits, plus 3 padded zeros at the highest bits. Therefore, it is given as 31 hexadecimal numbers, as shown in the example below. The bits are numbered as 0-123, from right to left.

078 2388 B808 7F80 0040 41B1 0005 c92c

Before the pre-adjustment, set the E-OCC and Em-OCC as 128 as described in subsubsection 2.2.4.

In the example data shown above, these 24 bits are within 7F80 004. For better explaination, it is expanded in binary form and those 24 bits are blacked out as shown below.

0111 1111 1000 0000 0000 0000 0100

Among these 24 bits, 18 bits of mode_data<72:55> consist of the thermometer code, as underlined below. They are used to coarsely adjust the frame mean. The more zeros, the lower the frame mean.

0111 1111 1000 0000 0000 0000 0100

The rest 6 bits, i.e., mode_data<78:73>, as underlined below, are used for fine adjustment of frame mean. The greater the code, the greater the frame mean.

0111 1111 1000 0000 0000 0000 0100

To adjust the frame mean, first use mode_data<72:55> to coarsely adjust the frame mean after power-up. If Vo is super-saturated, increase the number of zeros. If Vo is under-saturated, decrease the number of zeros. In this coarse adjustment, the change of Vo is usually big, which is normal. Then use mode_data<78:73> for fine adjustment. When the code changes from 00 0000 to 11 1111 gradually, the frame mean also increases along. Different bits in Vo_Sel<23:0> (mode_data<78:55>) are defined to carry different weights. Bits 0-17 carries weight 1. Bit 18 carries weight by 1/2, bit 19 by 1/4, and so on, up to bit 23, whose weight is 1/64.

Define P as the number of zeros in Vo_Sel<23:0>. The general rule is: the

greater is P, the smaller is the output.

Table 8: Typical configuration for analog output adjustment

Vo_Sel<23:0>(mode_data<78:55>)	P Value
0000 0 00 00 00 00 00 0 00 00 00 00	18.984375
1000 0 00 00 00 00 00 0 00 00 00 00	18.96875
1100 0 00 00 00 00 00 0 00 00 00 00	18.9375
1110 0 00 00 00 00 00 0 00 00 00 00	18.875
1111 0 00 00 00 00 00 0 00 00 00 00	18.75
1111 0 00 00 00 00 10 0 00 00 00 00	18.5
1111 0 00 00 00 00 11 0 00 00 00 00	18
1100 1 00 00 00 00 00 0 00 00 00 00	17.9375
1110 1 00 00 00 00 00 0 00 00 00 00	17.875
1111 1 00 00 00 00 00 0 00 00 00 00	17.75
1111 1 00 00 00 00 10 0 00 00 00 00	17.5
1111 1 00 00 00 00 11 0 00 00 00 00	17
1100 1 00 00 00 00 00 1 00 00 00 00	16.9375
1110 1 00 00 00 00 00 1 00 00 00 00	16.875
1111 1 00 00 00 00 00 1 00 00 00 00	16.75
1111 1 00 00 00 00 10 1 00 00 00 00	16.5
1111 1 00 00 00 00 11 1 00 00 00 00	16
1100 1 10 00 00 00 00 1 00 00 00 00	15.9375
1110 1 10 00 00 00 00 1 00 00 00 00	15.875
1111 1 10 00 00 00 00 1 00 00 00 00	15.75
1111 1 10 00 00 00 10 1 00 00 00 00	15.5

1111	1	10	00	00	00	15
11	1	00	00	00	00	
1111	1	11	00	00	00	14
11	1	00	00	00	00	

2.5.2 | EM-OCC ADJUSTMENT

After the preliminary adjustment, Vo still might deviate from the preset value. The user can adjust the Em-OCC for each row so that its mean value of Vo approaches the preset value (2.0V or 2.5V).

The general relationship between OCC code and Vo are listed in Tab.9. Now

Table 9: Relationship between OCC data and Vo

OCC change	Vo change
Em-OCC increase	Row mean Vo increase
E-OCC increase	Frame mean Vo decrease

set the E-OCC data of column 0-647 and Em-OCC data as 128 as described in

subsubsection 2.2.4. Read out the array output. Ideally, its row mean should be around the preset value. If the row mean is significantly greater or even super-saturated, lower the value of Em-OCC for this row. Otherwise increase it.

Even after Em-OCC adjustment, the row mean of Vo may still be super- or under-saturated. The user can just pick the configuration that gives the closest value, for the time being.

2.5.3 E-OCC ADJUSTMENT

Keep the Em-OCC data obtained in the previous step. The following procedures are used to get the E-OCC data of each individual pixel.

There are two common approaches to get the E-OCC code, successive approximation and brute force method. From experience, the former is better than the latter.

Listed below are the successive approaching procedure:

(1) In the beginning, E-OCC of each pixel is set as 128, then read out a frame of Vo, called as Vo1[i,j] (i for row and j for column).

(2) For those pixels whose Vo are higher than the preset value, add 1 to this pixel's E-OCC. For those pixel lower than the preset value, subtract 1 from its E-OCC.

(3) Send the new E-OCC, read out a frame of Vo after it is steady, called as Vo2.

(4) Compare Vo2 with the preset value and repeat (2)-(4) for 127 times. After this loop compare the 126^{th} and 127^{th} Vo with the preset value Vm. Save the E-OCC code that gives the closer result.

If Vo is still not ideal after this procedure, try changing the operation mode data mode_data<46:44> to modify the E-OCC precision and redo step (1)-(4).

This procedure is illustrated in the flowchart in Fig.9.

2.6 POWER ON AND POWER OFF

IR 03 18 X2A has an internal protection circuit to avoid improper power sequencing that leads to permanent damage. It is recommended that power on and power down should be carried out in accordance with Tab.10 and 11 to better protect the detector. The key point is to ensure that the bias voltage VSK, VREF and VEB are the last to power up and the first to power down.

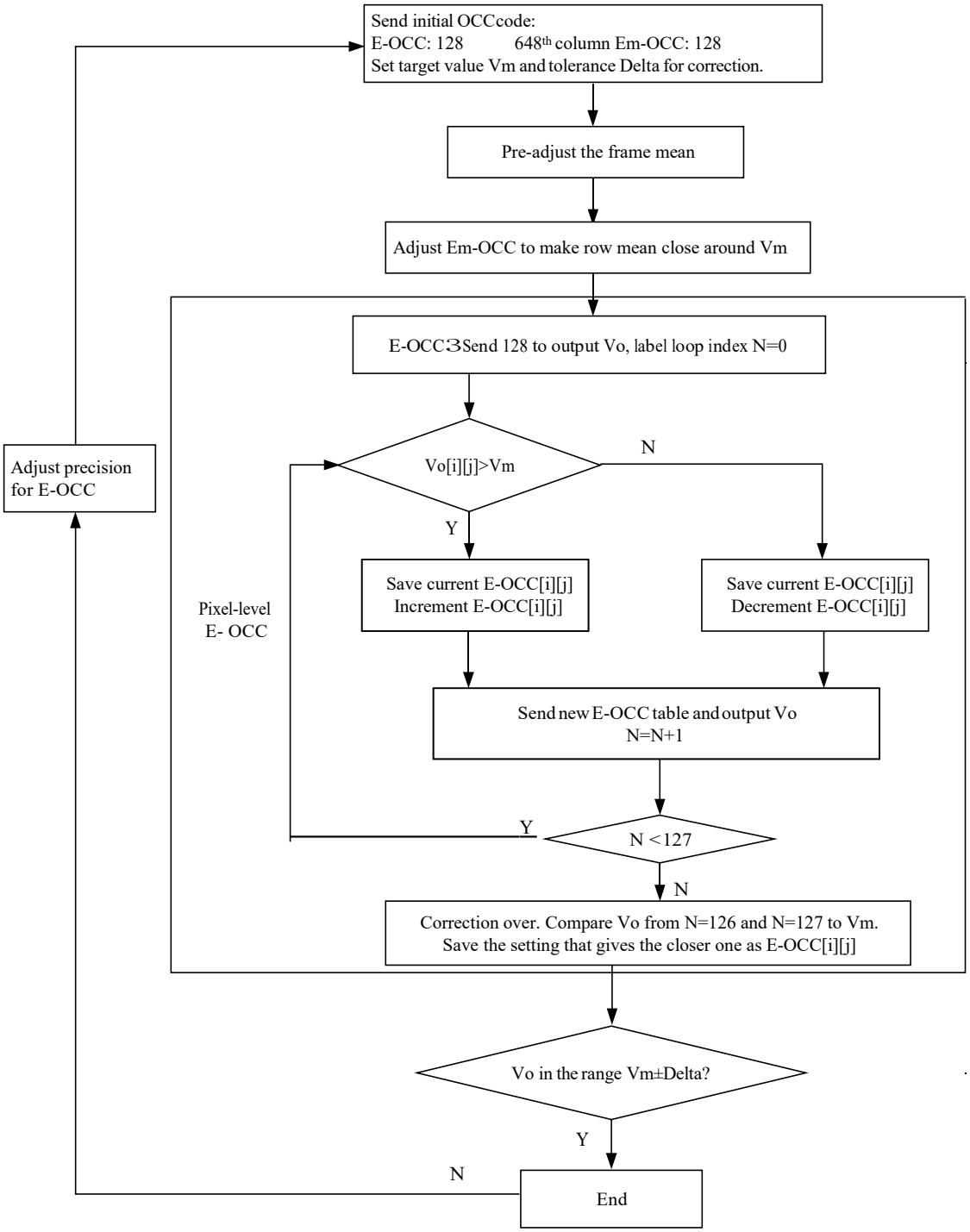

Figure 9: Successive approximation flow chart for OCC.

Table 10: Power up sequence

Sequence	Power up	Comments
1	VDDL_5V, VDDL	Enable detector digital supply rail
2	Digital Timing	Enable all detector timing
3	VDDA	Enable detector analog supply rail
4	VSK, VREF, VEB	Enable various pixel supply rail

Table 11: Power down sequence

Sequence	Power down	Comments
1	VSK, VREF, VEB	Disable various pixel supply rail
2	VDDA	Disable analog supply rail
3	Digital Timing	Disable detector timing
4	VDDL_5V, VDDL	Disable digital supply rail

3 THERMAL PARAMETER

3.1 OPERATION TEMPERATURE

IR 03 18 X2A detector can operate under -40^{o}C $\sim$ $+60^{o}$C. It is highly recommended to add a heat sink between the detector and the ambient to help heat dissipation, especially in a hot environment. Thermal resistance of the heat sink should be less than 4K/W. The heat sink can lower the TEC power as well.

3.2 STORAGE TEMPERATURE

Storage temperature for IR 03 18 X2A is -55^{o}C $\sim$ $+70^{o}$C.

3.3 WELDING TEMPERATURE

The welding temperature of IR 03 18 X2A is 350^{o}C for 10s.

3.4 FOCAL PLANE THERMOMETER

A temperature sensor is integrated inside the detector. The output from the analog pin VTEMP represents the real-time temperature of focal plane. VTEMP is calibrated during the manufacturing process. The analog voltage of VTEMP, with the slope +14.4mV/K, is around 2.5V $\pm$ 15mV when the focal plane temperature is 27 ^{o}C.

In general, VTEMP is the input of external TEC control circuit. To increase the stability of the TEC control loop, filtering and voltage dividing should be done before VTEMP is connected into the TEC control circuit as shown in Fig.10. It requires $R1 > 1M\Omega$ and $R2 = 4R1$. After the voltage dividing, the effective sensitivity of VTEMP is +2.88mV/K.

The R2 resistor in the figure could be removed. In this case the VTEMP is filtered and then connected to the TEC control loop.

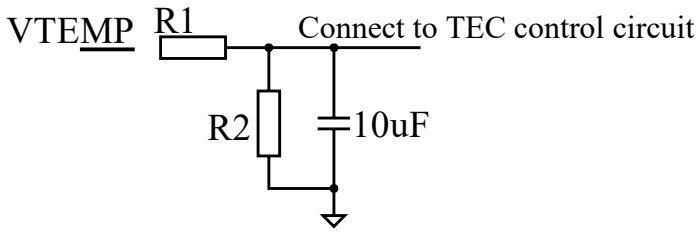

Figure 10: VTEMP filter circuit

4 ENVIRONMENT CONDITIONS

IR 03 18 X2A has passed rigid enviromental tests. The stress levels shown in Tab.12 do not represent the the highest level acceptable for the com- ponent but merely the qualification levels chosen by GWIC. Fig.11 shows the random vibration test condition.

Table 12: Thermal and mechanical test

Experiment	Standard	Method	Condition
HT storage	GJB-1788-1993	2020	T=70^{o}C, t=48h
LT storage	GJB-1788-1993	2040	T= –55^{o}C, t=24h
Random vibration	MIL-STD 883	2026	5.35g rms, 15minutes/axis, 3 axial direction 50 ~ 100Hz: +6dB/oct 100 ~ 1000Hz: 0.02g^{2}/Hz 1000 ~2000Hz: –6dB/oct
Mechanical shock	MIL-STD 810F	516.5	1/2 sine, 40g , 11ms 3 times per axis & per direc- tion.

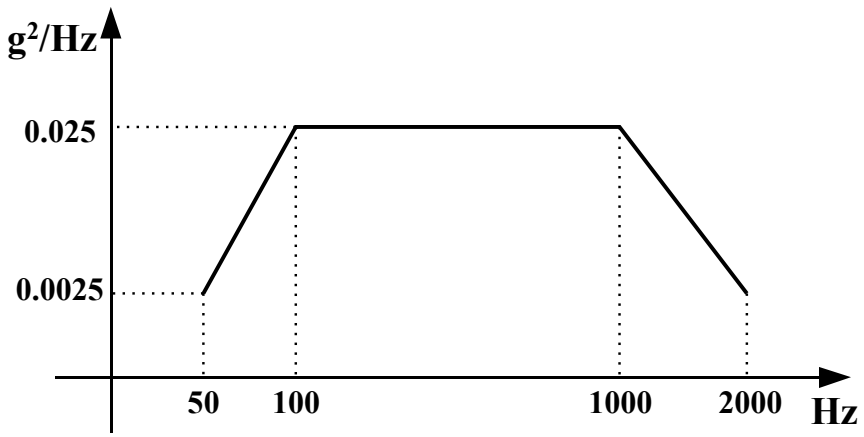

Figure 11: Random vibration test spectrum

5 | MECHANICAL INTERFACE

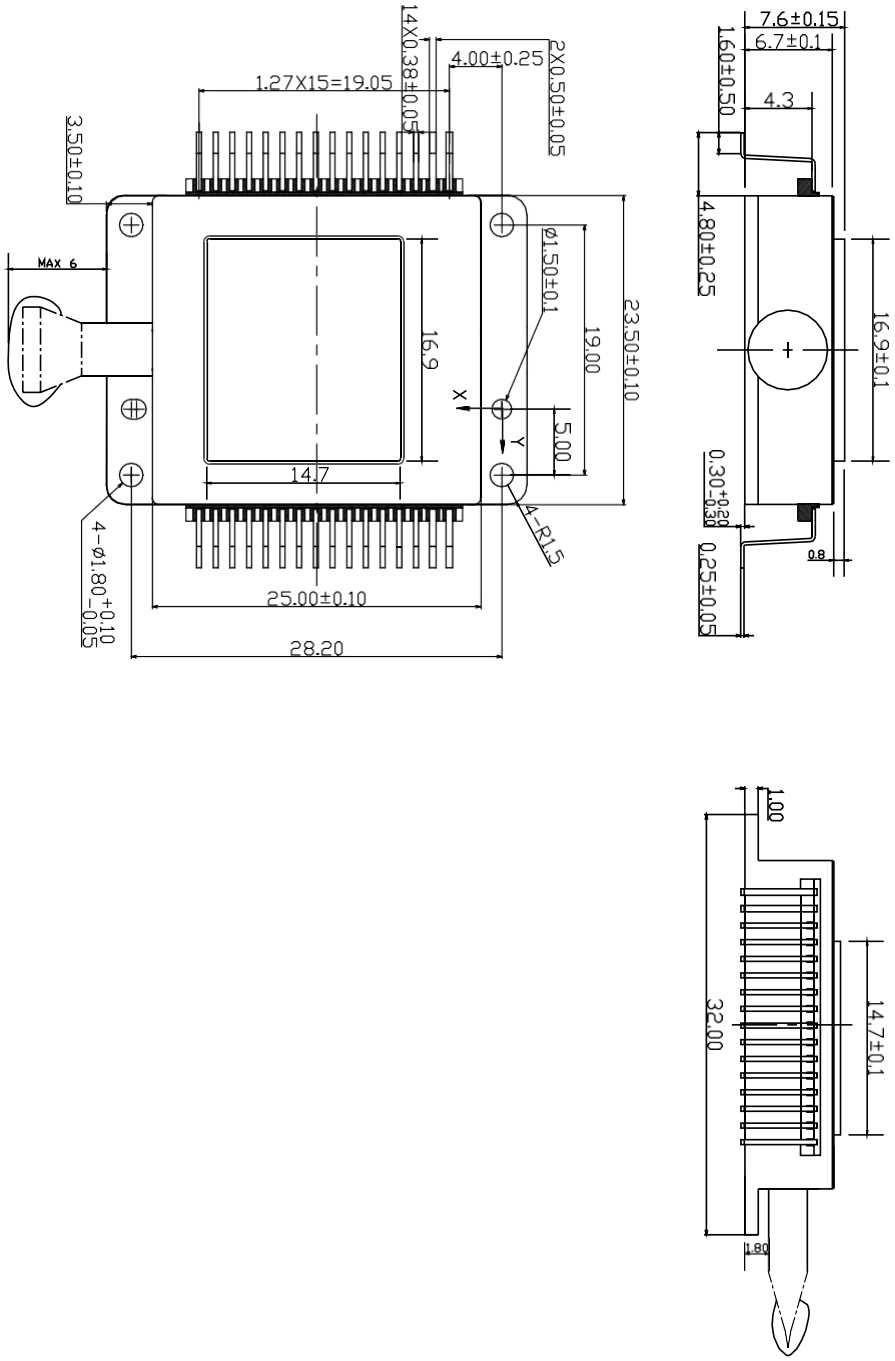

Figure 12: Mechanical drawing of IR 03 18 X2A

6 | OPTICAL INTERFACE

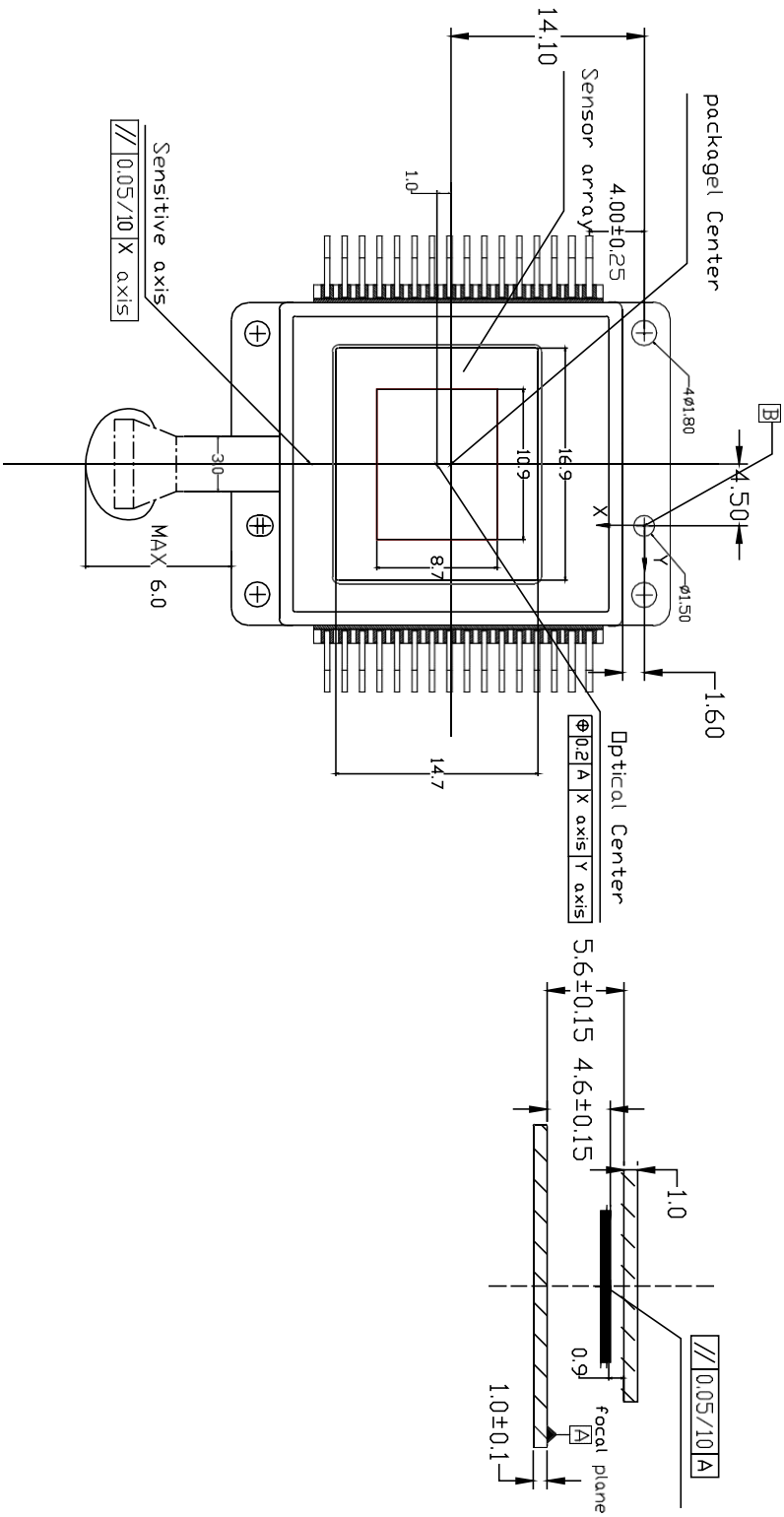

Figure 13: Optical alignment interface of IR 03 18 X2A

7 GLOSSARY

CTIA	Capacitance trans-impedance amplifier
Dummy	Blind pixel, which abosorbs radiation but its out put does not change.
FPA	Focal plane array
FS	Frame synchronization
GETTER	A getter is a kind of reactive material that is deliberately placed inside the housing to maintain the vacuum.
LWIR	Long wave infrared
MC	Master clock
NETD	Noise equivalent temperature difference
OCC	On chip correction
ROIC	Read-out integrated circuit
Sync	Synchronization
TEC	Thermoelectric cooler
T_{int}	Integration time
T_{line}	Line time
VREF	Reference voltage
VSK	Blind microbolometer bias
Vo	Analog output